Single phase system for detection of harmonic pollution sources at power grid

Dejan Stevanović, Predrag Petković and Volker Zerbe

Abstract: This paper present a system for harmonic source detection at power grid. It is implemented at Altera DE2 board. In combination with commercial power meter it represents powerful tool that allows utility to find each harmonic producer (nonlinear load). The base of this system is equation for distortion power calculation according to Budeanu definition. This equation showed up as the best indicator whether harmonic producer exists, or not at power grid. Measurement results that are obtained using this system at different type of light bulb confirmed our theory.

Key Words: Distortion power, FPGA, utility, detecting harmonic producer

I. INTRODUCTION

The last few decades are characterized by rapid development of electronics that changed the profile of the common customer's load. New electronic appliances characterize high sophistication, and high energy efficiency. Moreover, these devices reduce emission of carbon dioxide and bring smaller bill for consumed energy to customer. At first look everything looks great but that is not case. The main drawback of these devices is reach content of harmonics in load current, which cause many unwonted problems at utility and customer side [1], [2], [3]. These harmonics are result of the modern design of gadget. Namely, these devices operate at DC voltage while supplied from AC 230V RMS. Contemporary AC/DC converters are based on switching operation mode of transistors at frequencies up to several kHz. As result more power goes to the loads (electronic equipment) and less dissipate on AC/DC convertors. This has solved problem of energy efficiency but another problem aroused. All such loads, introduce harmonics at current. Increased number of AC/DC convertors connected to the power grid caused that the total distorted current reached very high level. Therefore, despite to the low resistance of power lines it jeopardizes the core of the power grid – integrity of the grid voltage. As result the utility faces the problem of increased loses [4], [5]. In order to save the system, many regulatory organizations brought standards that restrict the allowed amount of each harmonic. In order to save the system, many regulatory organizations brought standards that restrict the allowed amount of each harmonic. Two widely known standards in this area are the IEEE 519-1992 and IEC 61000 series. However, in these standards, there is no method and/or index defined for the detection of dominant harmonic sources. Many authors tried to find the best solution. Consequently many different methods are developed so far. Table I presents the state of art.

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TABLE I
THE STATE OF ART FOCUS ON THE HARMONIC SOURCE DETECTION AND SHARING HARMONIC RESPONSIBILITY METHOD

Method (Indices)	Required Data	Aims
Active Power Direction (APD)[6]	Voltage and current obtained by single point measurement	Harmonic Source Detection
Reactive Power Direction (RPD)[6]		
Nonactive Power Method (NP)[7],[8]		
Harmonic Polluted Ranking (HPR) method[9]	Current obtained by single point measurement	
Critical Impedance Method(CI)[10]	Thevenin's equivalents of utility and consumer sides	Sharing harmonic responsibility between utility and consumer

Our opinion is that a simple, inexpensive and applicable solution exists. It relies on efficient method for detection and measurement of harmonic pollution at the grid user's connection point. This paper will explain and demonstrate the solution in the following five sections.

The subsequent section describes the basic principle of operation electronic power meter. The third section explains the hardware realization of system for harmonic detection source at power grid. The measured results are presented in fourth section before conclusion.

II. THE THEORY OF OPERATION OF ELECTRONIC POWER METERS

The core of each electronic power meters is a chip which calculates all power quantities that are of interest for utility to control consumption and create bills. Usually these values are defined by appropriate standard. All these circuits relay on digital signal processing of voltage and current samples. The instantaneous value of voltage and current are attenuated through voltage divider and current transformers respectively. The obtained signal at output of attenuator is sent to ADC where is sampled at discrete

time points (at least two per a period, according to the Nyquist-Shannon theorem) and digitalized. DSP processes digital voltage and current samples and calculate all necessary power quantities. Instantaneous value of signal (current or voltage) in time domain can be express as:

$$x(t) = \sqrt{2} X_{RMS} \cdot \cos(2\pi f t + \varphi) \ . \quad (1)$$

After the discretization in equidistant time intervals it transforms to:

$$x(nT) = \sqrt{2} X_{RMS} \cdot \cos(2\pi \frac{f}{f_{sempl}} n + \varphi) \ , \quad (2)$$

where f and f_{sempl}, are frequency of the signal and the sampling frequency. The RMS value is calculated using the following equation:

$$X_{RMS} = \sqrt{\frac{\sum_{n=1}^{N} x(nT)^2}{N}} \ . \quad (3)$$

The active power is obtained as average of the instantaneous multiplication of instantaneous values for current and voltage, and average active power one gets in form:

$$P = \frac{\sum_{n=1}^{N} v(nT) i(nT)}{N} = \frac{\sum_{n=1}^{N} p(nT)}{N} . \quad (4)$$

The same equationis used for reactive power calculations, only difference is in voltage samples that are shifted for $\pi/2$.

In addition, apparent power S can be calculatedas the product of RMS voltage and current values.

$$S = V_{RMS} \cdot I_{RMS} \quad (5)$$

Some level of error in active and reactive power calculation is possible. This error is caused due to phase difference between voltage and current and the fact that the power line frequency is slightly changed around the nominal (50Hz). These errors can be eliminated/diminished by additional calibration and correction within appropriate filters.

Once when P is calculated according to Eq. (4), Q calculated on similar way using shifted voltage samples, and apparent power S obtained using (5) one easily can compute distortion power using Budeanu's definition:

$$D = \sqrt{S^2 - P^2 - Q^2} \ . \quad (6)$$

Unfortunately the existing regulation did not require that power meter calculate component of apparent power. Therefore direct implementation of Eq. (6) for distortion power is not possible for most commertialy available meters.

Despite some arguing about the accuracy of Eq. (6), up today it only has real practical application. All other are too complicated to be implemented at comercial level. In practice many authors confirmed that the value of distortion power defined with Eq. (6) directly follows total harmonic distortion of current [11]. As stated at beginning, harmonic cause many unwonted problems at customer and utility side. If one wants to reduce the level of harmonic he needs an instrument to measure them. It would be very convenient if the instrument could use measured by commercial electronic power meter. The following section will describe our solution.

III. System for Detection Source of Harmonic Pollution at Power Grid

So far there several methods for harmonic source detection at power grid are published [6], [7], [8], [9], [10]. Neither of them can give precise information about the pollution produced by a single customer. That is one of the main drawbacks of already existed methods. Moreover, these methods cannot be easily implemented at ordinary power meter. Therefore we were inspired to offer our solution that is based on Eq. (6). As we show in some of previously published papers [12], the value of distortion power is good indicator of existing harmonic source at grid. Bearing in mind the expenses of chip redesign and/or modification of power meters in service, we suggest an upgrade that could be easily fitted into existing power meters. Hence our idea is to realize hardware that can be implemented as a dongle for all electronic meters without change in their construction. Namely on this way we will just connected our system at the power meter. This system is implemented at Altera DE2 board with Altera Cyclone® II 2C35 FPGA. The block diagram of realized system is shown in Fig. 1. It consists of RS232 interface, RAM, ROM, two address generator blocks for both type of memory, FSM, and circuit for power distortion calculation. The data manage transfer is controlled by FSM. ROM memory is used to memorize commands that are sent to power meter, while RAM is used to memorize received data.

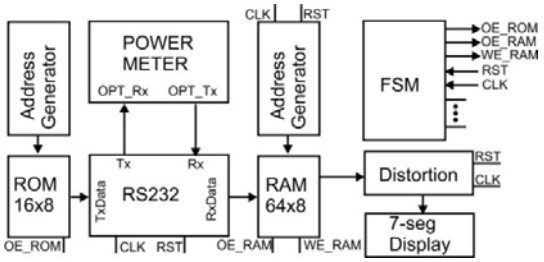

Fig.1. Block diagram of realized system

The communication between Altera DE2 board, where system is realized, and power meter is done through RS232 and optical port. Communication is done in two steps. In the first step the system sends command that require data for voltage and current from power meter and saves them in RAM memory. Then system requires and stores data for active and reactive power. All received data come in BCD format. Therefore it is necessary to convert them in HEX format using *Shift and Sub-3 Algorithm* and extended to words 24 bit long. The theory of the conversion algorithm is simple: divide 24 bit numbers in 4-bits numbers that presents the hundreds thousands, tens thousands, thousands, hundreds, tens, and units. After that check if they are greater or equal to 8, then subtract 3 from it. After that, shift the binary number right by one bit. Finally we repeat the process 24 times.

A. RS232 Interface

The RS232 is the widely used asynchronous serial wire interface brought by Electronic Industries Association (EIA) for the interchange of data between two devices. It was initially developed by the EIA to standardize the connection of computers with telephone line modems and letter became inevitable part of electronic equipment. Moreover it becomes standard communication protocol integrated inside processors and microcontrollers. This interface works in combination with UART universal asynchronous receiver/transmitter. When transmitting a byte, the UART (serial port) first sends a START BIT which is a positive voltage (0), followed by the data (generally 8 bits, but could be 5, 6, 7, or 8 bits) followed by one or two STOP BITs which is a negative(1) voltage. The RS-232 standard specifies that logic "1" is to be sent as a voltage in the range -15 to -5 V and that logic "0" is to sent as a voltage in the range +5 to +15 V. This standard defines that voltage with amplitude of at least 3 V will always be recognized correctly at the receiver according to their polarity. Therefore it tolerates appreciable attenuation along transmission line. The waveform of transmitted signal at UART Tx pin is shown in Fig. 2.

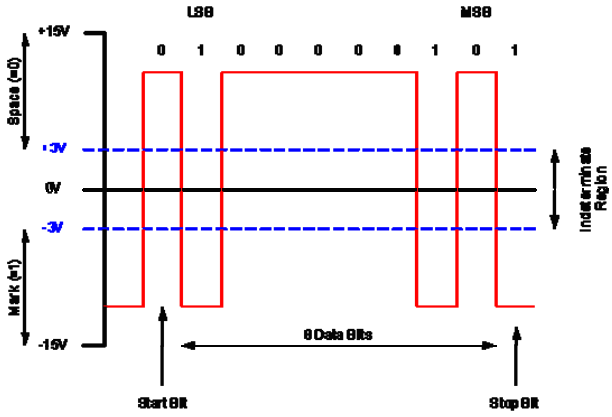

Fig.2 shows a waveform of transmitted byte

The baud rate of the sent word is device-dependent. It is usually in range from 300 to 230400 bit/s. The structure of realized RS232 interface is very simply. It is based on two shift register: The first shift register accepts the input data at TxData(7:0) port and automatically serialize and emit the byte on the Tx pin. During emitting data at Txpin, pin IntTx is reset to indicate that transmitting is not complete. Therefore a rising edge on IntTx_O can trigger the interrupt line of a microcontroller to emit another byte. The second shift register un-serialize data received on Rx pin. When the received bit stream is un-serialized the IntR pin is set. This announces that the received byte can be read on the data output bus RxData. As soon as the byte is read, IntRx is reset.

B. Distortion power calculation

The block diagram of circuit for power distortion calculation is shown in Fig. 3. Note that this part of VHDL code can be used as a predesigned IP core ready to be embedded into integrated power meter IC.

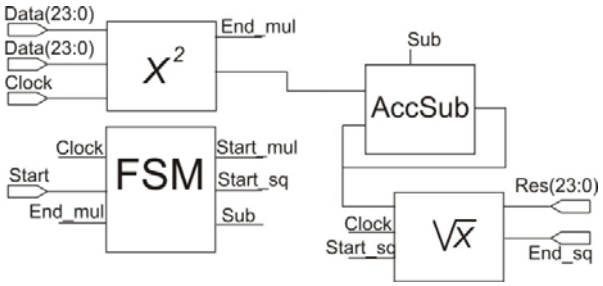

Fig.3. Block diagram of circuit for power distortion calculation

The serial multiplier successively accepts 24-bit wide values of active, reactive and apparent power from 24 bits registers. This multiplier is realized using iterative method. The proposed algorithm is very fast and its hardware implementation has small chip area. For the whole process of multiplication it needs the number of clock pulses that equals length of operands in bits. After multiplication AddSub block adds squared values of P^2 and Q^2 and subtract it from S^2. Eventually the square root block calculates D.

The circuit for square root computation is realized using iterative method or Longhand square root computation method. This algorithm is very fast and its hardware implementation requires small chip area. The algorithm computes square root on the same way like people do manually. The detail information about realization of this circuit can be found in [13].

IV. Results of Measuring

The hardware of the realized system is verified using a set of different energy saving light bulbs. They are chosen as benchmarks for simple nonlinear loads that characterize

small nominal power. Namely the intention is to show that small numbers that may appear after subtracting in Eq. (6) did not play important role for nonlinear load detection. This is due to the good resolution of data provided by the standard electronic power meter.

Fig.4 illustrates how the implemented system operates in conjunction with ordinary electronic power meter. This meter is produced by EWG electronics [14]. It fulfills the standard IEC 62052-11 [15].Note that this meter already provides I_{RMS}, V_{RMS}, P and Q_B, according to Eq. (3) and Eq. (4), respectively. The data from power meter are read using its optical head (optical port) and transmitted to Altera DE2 board trough the RS232 port. Then after, calculating D_B as stated by Eq. (6) is straightforward. The developed hardware is compatible with a wide range of other power meters that meet similar specifications regarding standards, type of output data and optical port.

Table II summarizes obtained results of measuring collected from the meter (V_{RMS}, I_{RMS}, P, Q_B) and provided by the proposed dongle (S and D_B). The value of distortion power that is calculated at FPGA on Altera DE2 board appears on seven segment display as illustrated in Fig.4.

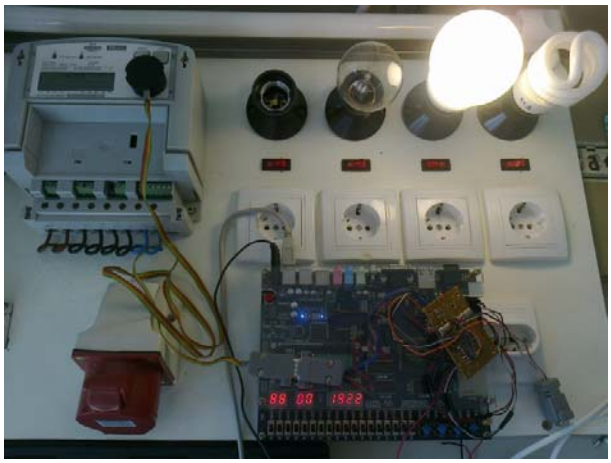

Fig4. Realized system for distortion power measurement

TABLE II
RESULT OF MEASUREMENT

Loads	U_{RMS}	I_{RMS}	S	P	Q_B	D_B	D_B/S[%]	D_B/P[%]
Incandescent lamp 100W	218.96	0.42	91.96	91.96	0.74	0.00	0.00	0.00
FL18W	218.62	0.08	17.49	11.33	-5.80	11.99	68.58	105.83
CFL20Wbulb	218.55	0.13	29.07	18.30	-8.81	20.79	71.54	113.61
CFL 20Whelix	219.01	0.14	30.66	18.61	-9.38	22.49	73.35	120.85
CFL 20Wtube	219.46	0.14	31.60	18.73	-9.58	23.58	74.62	125.89
CFL 15Wbulb	219.74	0.09	19.56	12.10	-5.51	14.34	73.34	118.51
CFL 11Whelix	221.73	0.08	17.74	10.42	-5.38	13.31	75.03	127.74
CFL 11Wtube	221.27	0.08	17.92	10.76	5.74	13.13	73.28	122.03
CFL 11WE14	215.51	0.08	17.24	10.79	-5.26	12.38	71.78	114.74
CFL 9Wbulb	216.06	0.06	12.75	7.58	-3.64	9.58	75.16	126.39
CFL 7Wspot	217.75	0.04	9.58	5.83	-2.87	7.04	73.48	120.75
CFL 7W	219.83	0.04	9.67	6.03	-2.57	7.11	73.54	117.91
CFL 15Whelix	218.55	0.15	32.13	18.95	-10.26	23.83	74.17	125.75
CFL 20Wtube	216.91	0.11	24.08	13.86	-7.15	18.34	76.19	132.32
LED Parlamp 15W(9x1.5W)	217.27	0.157	34.11	16.9	-3.87	29.38	86.12	173.85
LED Parlamp(6x1.5W)	217.51	0.114	24.80	12.89	-2.74	21.00	84.71	162.92
LED Bulb(7x1W) Warm White	218.02	0.083	18.10	9.7	-2.84	15.01	82.95	154.74
LED Bulb(6x1W) Warm White	217.93	0.042	9.15	7.76	-0.14	4.85	53.00	62.50
LED Bulb(6x1W)White	217.85	0.045	9.80	8.34	-0.16	5.15	52.53	61.75
LED Bulb 3x1W	217.9	0.034	7.4086	3.96	-0.89	6.20	83.66	156.57
LED MiniBulb3x1W	215.86	0.034	7.33924	3.91	-1	6.13	83.52	156.78

Once when the utility is able to register the level of distortion power at Point of Common Coupling (PCC) it could provide better control at the grid. The controlling mechanism may be explored through the billing policy or by disconnection of large nonlinear loads. The first will reduce losses caused by the lack of ability to measure considerable part of the supplied energy. The second could be activated to protect other consumers from irresponsible users.

V. CONCLUSION

This paper presented a single-phase system that can be used for detection each source of harmonic pollution at power grid. It can be implemented in on-shelf power meter. The advantaged of this system is the fact that can be used as a dongle without any changes at power meter. Practically in many countries old electrical power meters have recently been replaced by electronic meters. However all of them are not able to register distortion power that in contemporary households and offices arise to values that cannot be ignored. The result from Table II indicated that utility suffers large losses due to the lack of registering distortion power. In cases of most energy saving light bulbs it is greater than registered active power. As we have recently published in [4], [5] measuring distortion power at PCC helps the utility to eliminate losses. Therefore there is a need to attach an additional inexpensive hardware that will operate in conjunction with existing meters and upgrade their possibilities. The realized system allows utility to detect and quantify the level of pollution from each customers, what makes the proposed system unique.

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